National Aeronautics and Space Administration

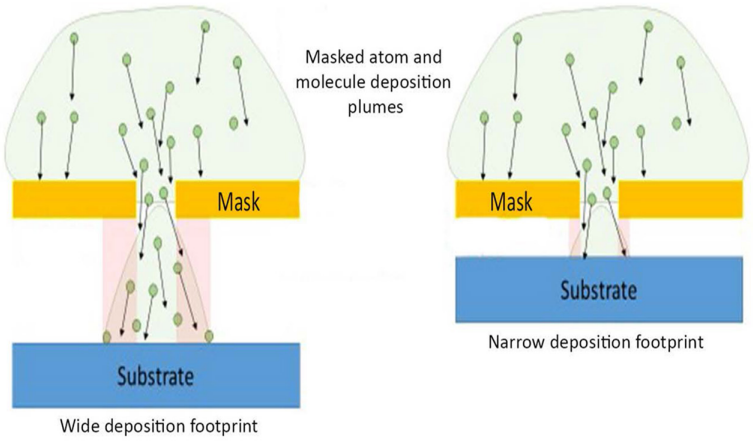


Image Credit: NASA

TECHNOLOGY SOLUTION

Manufacturing

Simplified Complimentary Metal-oxide-semiconductor Manufacturing Technique

Unique deposition process for CMOS manufacturing eliminating photoresists, UV exposure and other steps - Applicable for 3D transistors

Current microfabrication methods are well established for processing of Si-based complementary metal-oxide-semiconductor (CMOS) and only get more complex with each iteration. This is especially true with 3D transistors that require very selective placement and selective removal of materials required to reach a working product.

However, with NASA's newly developed masking and deposition processes, photoresists, UV exposures and selective etching can be eliminated, with metal removal reduced to only planarization. This revised process reduces the total material and time requirements drastically when compared to current standards.

These advancements offer the benefits of increasing total possible throughput while simultaneously reducing manufacturing cost per unit.

BENEFITS

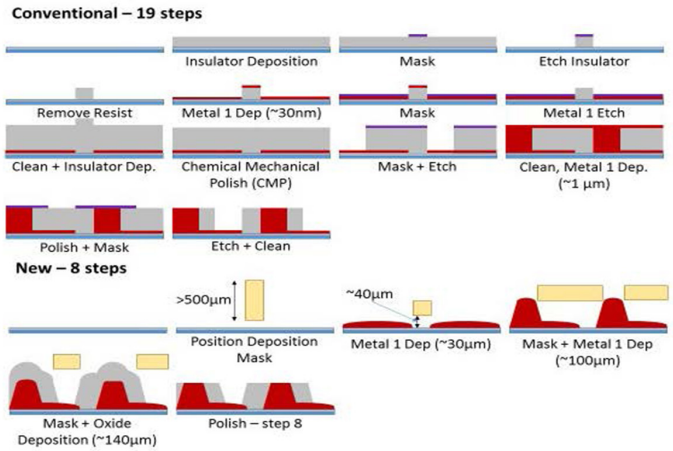
- Shortens the patterning process for deposition, skipping the need for photoresist and UV exposure
- Cost is reduced
- Environmental impact is reduced from less chemical disposal
- Less material waste from etching away undesirable deposition
- Most effective for fabrication process for group III-V and II-VI semiconductors which do not have proper gate oxides
- Effective for thick film processing

THE TECHNOLOGY

This innovation represents an alternative method to skip several of the conventional fabrication steps, using a mask designed to allow molecules in a sputtering plume to pass through openings engineered in the mask. This causes material to go where desired, without photoresist, and without selective etching, thus simplifying the process, reducing cost, chemical waste; and increasing throughput.

This method masks areas that do not need deposited material, causing local deposition instead. The shape and size are within tolerance. No etching steps, no photoresist patterning, and no metal removal is necessary. Other than planarization, selective deposition has replaced every step in the conventional process, accomplishing the same result in 8 steps instead of 19.

The technology can be easily used to fabricate custom chips and specialized sensors and devices that use the group III-V and II - VI semiconductor materials.



Comparison of the conventional & new processes. Image Credit: NASA

APPLICATIONS

The technology has several potential applications:

- Semiconductors
- Computer equipment
- Telecommunications equipment
- Wireless communications
- Automotive applications
- Electronic imaging / optoelectronics
- Medical imaging

PUBLICATIONS

Patent No: 10,886,452; 11,581,468

technology.nasa.gov

NASA's Technology Transfer Program pursues the widest possible applications of agency technology to benefit US citizens. Through partnerships and licensing agreements with industry, the program ensures that NASA's investments in pioneering research find secondary uses that benefit the economy, create jobs, and improve quality of life.

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More Information

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